Amendments to the Claims

1. (currently amended): An electronic device package comprising:

a support substrate including a flag, wherein the flag has a bonding surface;

a first electronic chip having a first peripheral edge, wherein the first electronic chip is attached to a first portion of the bonding surface with a first die attach material;

a first continuous trench formed in the flag in proximity to the first peripheral edge, wherein the first continuous trench includes ~~a curved sidewall surface~~ a continuously rounded cross-sectional shape and an inner edge adjacent to the first peripheral edge, and wherein the first continuous trench surrounds the first electronic chip; and

an encapsulant covering the first electronic chip and at least a portion of the curved sidewall surface.

2. (currently amended): The package of claim 1, wherein first continuous trench has a width greater than about 50 microns ~~the first continuous trench surrounds the first electronic chip.~~

3. (currently amended): The package of claim 1, wherein the first continuous trench has a width between about 102 microns and about 330 microns. ~~comprises a continuously rounded cross-sectional shape.~~

4. (original): The package of claim 1, wherein the first continuous trench has a cross-sectional shape comprising an inverse omega shape.

5. (original): The package of claim 1, wherein the first continuous trench has a rounded corner.

6. (original): The package of claim 1, wherein the first

continuous trench has depth in range from about 100 microns to about 330 microns.

7. (withdrawn): The package of claim 1, wherein the peripheral edge is substantially aligned with the inner edge of the first continuous trench.

8. (original): The package of claim 1, wherein the first peripheral edge is spaced a distance inside the inner edge of the first continuous trench.

9. (original): The package of claim 8, wherein the distance is less than about 635 microns.

10. (withdrawn): The package of claim 1, wherein the first peripheral edge extends over the inner edge of the first continuous trench.

11. (original): The package of claim 1, wherein at least a portion of the first die attach material extends to the inner edge of the first continuous trench, and wherein the first continuous trench is substantially absent die attach material.

12. (withdrawn): The package of claim 1 further comprising a second trench formed in the flag, wherein the first electronic chip overlies at least a portion of the second trench.

13. (original): The package of claim 1, wherein the die attach material is selected from a group consisting of a eutectic solder, a solder paste, a conductive epoxy, a polyimide film, a metal filled glass, and a pre-form structure.

14. (withdrawn): The package of claim 1 further comprising:

a second electronic chip having a second peripheral edge, wherein the second electronic chip is attached to a second portion of the bonding surface with a second die attach material; and

a second continuous trench formed in the flag in proximity to the second peripheral edge and around at least two sides of the second electronic chip, wherein the second continuous trench includes a curved sidewall surface adjacent the second peripheral edge.

15. (withdrawn): The package of claim 14 wherein the first and second continuous trenches have a common portion.

16. (withdrawn): The package of claim 14 wherein the first and second die attach materials comprise different materials.

17. (original): The package of claim 1, wherein the support substrate further includes a bonding site having a bonding surface, and wherein the package further comprises a bonding device coupling the first electronic chip to the bonding site, wherein the encapsulant covers the bonding device and the bonding surface of the bonding site.

18. (original): The package of claim 1, wherein the first continuous trench comprises an etched trench.

19. (withdrawn): A method for forming an electronic device package comprising the steps of:

providing a support substrate comprising a flag and a first trench formed in a bonding surface of the flag, wherein the first trench has a cross-sectional shape including a curved sidewall surface;

attaching a first electronic chip having a first peripheral edge to the bonding surface with a die attach material, wherein the first trench is in proximity to the first peripheral edge, and wherein the curved sidewall surface is adjacent the first peripheral edge; and

covering the first electronic chip and portions of the flag with a protective layer, wherein the protective layer covers at least a portion of the curved sidewall surface.

20. (withdrawn): The method of claim 19 wherein the step of providing the support substrate includes providing a support substrate having a first trench that surrounds the first peripheral edge.

21. (withdrawn): The method of claim 19 wherein the step of providing the support substrate includes providing a support substrate having a first trench, wherein the first trench has a continuously rounded cross-sectional shape.

22. (withdrawn): The method of claim 19 wherein the step of attaching the first electronic chip to the bonding surface comprises the steps of:

placing the die attach material on a portion of the bonding surface bounded by the first trench; and

placing the first electronic chip on the die attach material, wherein the first trench prevents the die attach material from spreading beyond an inner edge of the first trench to align the first electronic chip on the bonding surface.

23. (withdrawn): The method of claim 19 wherein the step of covering comprises encapsulating the first electronic chip and portion portions of the flag with a plastic encapsulant, wherein the plastic encapsulant extends into the first trench to provide a mold lock.

24. (withdrawn): The method of claim 19 wherein the step of placing the first electronic chip includes substantially aligning the first peripheral edge with an inner edge of the first trench.

25. (withdrawn): The method of claim 19 wherein the step of placing the first electronic chip includes placing the first electronic chip wherein the first peripheral edge is spaced a distance inside an inner edge of the first trench.

26. (withdrawn): The method of claim 25 wherein the step of placing the first electronic chip includes placing the first electronic chip a distance less than about 635 microns from the inner edge of the first trench.

27. (withdrawn): The method of claim 19 wherein the step of placing the first electronic chip includes placing the first electronic chip wherein the first peripheral edge extends over an inner edge of the first trench.

28. (withdrawn): The method of claim 19 wherein the step of providing the support substrate includes the steps of:

providing a leadframe having the flag with the bonding surface;

masking the bonding surface to form a masking layer;

selectively removing portions of the masking layer to expose portions of the bonding surface; and

etching the first trench into the bonding surface to provide the curved sidewall surface.

29. (withdrawn): The method of claim 28 wherein the etching step includes etching the first trench to provide an inverse omega cross-sectional shape.

30. (withdrawn): The method of claim 19 wherein the step of providing the support substrate includes providing a support substrate having a second trench formed in the bonding surface, wherein the second trench has a cross-section shape including curved sidewall surfaces.

31. (withdrawn): The method of claim 30 further comprising the steps of:

attaching a second electronic chip having a second peripheral edge to the bonding surface with a second die attach material, wherein the second trench is in proximity to the second peripheral edge; and

covering the second electronic chip and at least a portion of the curved sidewall surfaces of the second trench.

32. (withdrawn): The method of claim 30 wherein the step of providing the support substrate includes providing the support substrate wherein the first and second trenches have a common portion.

33. (original): A leadless electronic structure comprising:

a leadframe including a bonding site and a flag having a bonding surface;

a first semiconductor device having a first peripheral edge coupled to the bonding surface with a first chip attach layer, wherein the first semiconductor device includes a bond pad;

a first groove formed in the bonding surface surrounding the first semiconductor device, wherein the first groove comprises a substantially continuously curved inner surface and a first inner edge in proximity to the first peripheral edge, wherein at least a portion of first chip attach layer extends across the bonding surface and terminates at approximately the first inner edge;

a bonding device coupling the bond pad to the bonding site; and

an encapsulating layer covering exposed portions of the flag, the bonding site, and the bonding device, the first semiconductor device, and at least a portion of the substantially continuously curved inner surface.

34. (original): The structure of claim 33 further comprising:

an electronic device having a second peripheral edge coupled to the bonding surface with a second chip attach layer; and

a second groove formed in the bonding surface surrounding the electronic device, wherein the second groove comprises a substantially continuously curved inner surface and a second inner edge in proximity to the second peripheral edge, and wherein at least a portion of the second chip attach layer extends across the bonding surface and terminates at approximately the second inner edge.

35. (original): The structure of claim 33 wherein the first chip attach layer comprises a conductive solder.

36. (original): The structure of claim 33 wherein the first peripheral edge is placed an inner distance from the first inner edge.

37. (original): The structure of claim 36 wherein the inner distance is less than about 635 microns.

38. (original): The structure of claim 33 wherein the first peripheral edge is substantially aligned with the first inner edge.

39. (original): The structure of claim 33 further comprising a shaped trench formed in the bonding surface, wherein the first semiconductor device overlies at least a portion of the shaped trench.

40. (original): The structure of claim 39 wherein the shaped trench comprises a cross shape.

41. (original): The structure of claim 39 wherein the shaped trench is connected to the first groove.

42. (original): The structure of claim 33 wherein the first groove includes a rounded corner.